What is claimed is:

1   1.   A single bit FIR filter comprising:

2   an input adapted to receive a plurality of serial input bits, said input bits being a single

3   bit wide; said input comprising a predetermined number of input nodes; said input nodes separated

4   into one or more sets of input nodes; said input adapted to allow said plurality of input bits to shift

5   down the length of said input;

6   a storage device having a plurality of memory locations, each said memory location

7   having an address such that bits in a first set of input nodes can be utilized to address one of said

8   memory locations;

9   an output providing an accumulation of the contents of said the memory locations that

10   were addressed.

1   2.   The single bit FIR filter of claim 1, wherein said input has a single set of input nodes.

1   3.   The single bit FIR filter of claim 1, wherein said input further comprises a second set

2   of input nodes such that bits in said second set of input nodes can be utilized to address a second one

3   of said memory locations, said output providing an accumulation of the contents of first and said

4   second memory locations.

1   4.   The single bit FIR filter of claim 1 further comprising an accumulator for receiving

2   the contents of said addressed memory locations such that the output of said single bit FIR filter is an

3   accumulation of the contents of said addressed memory locations.

1   5.   A single bit FIR filter for comprising:

2   an input portion for receiving a stream of serial input bits, said input portion

3   comprising a plurality of input node sets, each said input node set is for receiving input bits from said

4   serial stream of input bits;

5   a memory comprising memory locations having an address and a value, said memory

6   locations adapted to be addressed indirectly or directly by the contents at least one of said input node

7   sets

8   an accumulator adapted to receive the contents of said addressed memory locations;

9   said accumulator adding said contents of said addressed memory locations and producing a result;

10   said result being substantially an output of said single bit FIR filter.

1   6.   The single bit FIR filter of claim 5, wherein said memory locations are addressed

2   indirectly by having said contents of a first input node set be subjected to an address offset prior to

3   being provided to said memory.

1   7.   The single bit FIR filter of claim 5, wherein each input node set comprises the same

2   number of input nodes.

1   8.   The single bit FIR filter of claim 5, wherein said input node sets comprise shift

2   registers.

1   9.   A method for providing a single bit FIR filter comprising:

2   receiving serial data into an input, said input being divided into sets of input data;

3   using each set of input data to directly or indirectly address memory locations

4   associated with each set of input data;

5   reading the contents of said addressed memory locations;

6   accumulating the contents of said addressed memory locations

7   providing a single bit FIR filter output.

8   10.   The method of claim 9 further comprising, after said using step, shifting said input

9   data at least one input data position.

1   11.   The method of claim 9 further comprising shifting said input data at least one input

2   data position and after said step of providing repeating said method starting at said step of receiving.

1   12.   The method of claim 9 further comprising loading said memory locations with values

2   prior to the step of receiving.

1   13.   The method of claim 9, wherein each set of input data comprises the same number of

2   input bits.

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1   14.   A method of providing a single bit FIR filter comprising:

2   inputting a first bit of a serial stream of data into an input portion;

3   dividing said input portion into sets of data that can be used to address a memory

4 directly or indirectly;

5   addressing a memory location of said memory with at least one set of data;

6   reading the contents of said memory location;

7   accumulating the contents of said memory location with the contents of other memory

8 locations; and

9   providing an output of said accumulator as an output.

1   15.   The method of claim 14, wherein each said set of data can be adapted to be used as an

2 address.

1   16   The method of claim 14, wherein a set of data can be used to address a memory

2 indirectly by providing said set of data with an offset.

1   17.   The method of claim 14 wherein said input portion is at least on of 8, 16, 32, 64, or

2 128 bits long.